REMARKS/ARGUMENTS

Applicant responds herein to the Office Action dated June 30, 2003.

Claims 1-3 and 5-13 stand rejected on grounds of obviousness over Nakamura (5,627,583), in view of Yabe (4,845,555). Claim 4 is stated to be obvious over Nakamura and Yabe, further in view of Pasqualini (6,397,374 B1). Reconsideration is requested in view of the amendments to the claims herein and the following remarks.

As described in the introductory pages of the instant specification, the need for, and the advantage derived from correcting endoscope signals for signal line delays are known.

The present invention focuses on achieving a modular, more widely applicable solution that fits a large diversity endoscope devices.

Accordingly, the present invention has evolved and presents for patenting, a delay circuit scheme in which the delay circuitry is made part of the signal processing microprocessor and is furthermore, programmable in a way that it can be used with a variety of endoscopes, without requiring special arrangements or hardware for different endoscopes that might be connected to the basic operational and signal processing circuit.

With reference to Figure 1 (which is being utilized to explain, rather than to limit, the claims), the output of signal source 32, is routed through the delay circuit 33 and then is provided to the CCD drive circuit generator, which then produces the signal that is supplied to a driver that provides the amplified or conditioned signal to actual endoscope hardware.

A portion of the same delay circuit 33 is utilized at the receiving end, to process the return signal, to appropriately delay it and synchronize it in order to avoid the fundamental problem of signal line delays, as discussed in the instant specification.

With specific reference to claim 1, as amended, there is recited a signal source, as well as a drive signal generator for driving an imaging device, e.g., a CCD, and a delay circuit.

Apart from the recitation that the delay circuit is included as part of the first processor, claim 1 further specifies that the delay circuit is interposed at least partially between the signal source and the first drive signal generator.

The specific arrangement of the delay circuit of the present invention as part of the "first processor" reduces the overall number of components that are typically necessary and increases

the versatility and usability of the device, since the delay circuit can be programmed as part of the processor to accommodate a great variety of endoscopes.

Note further that in claim 1, the delay circuit is effective for delaying at least part of the signals that are included in both "the first drive signal" and "the second drive signal."

Turning to the references, it is respectfully submitted that, even in combination, the cited references do not disclose or suggest the invention of claim 1. In the primary Nakamura reference, the Examiner mentions the delay circuit 91, which is shown in Figure 8 of that reference. That delay circuit 91 is referenced, and the function thereof is explained, at column 9, lines 41-55 of Nakamura. It is very evident that this reference does not at all discuss the signal line delays which are at the heart of the present invention. The delay circuit 91 is used to obtain color difference signals of 2R-G and 2B-G. They do not appear to be associated with the functionality of the present invention. Indeed, the 1H delay circuit 91 does not appear to have any nexus to any functionality involving delaying the CCD driving signal that is obtained from the driver 82 in this reference.

Further, with respect to the primary Nakamura reference, the Office Action itself concedes that no delay circuit is disclosed which is part of the first processor of the present invention. Accordingly, the Office Action has turned to the secondary reference, namely Yabe, for the proposition that it teaches a delay circuit embedded in the "first processor."

In Figure 1 of Yabe, the timing switching circuit 18 drives the timing generator 17, which in turn drives the sample and hold circuit 16. This circuit is obviously not related to the CCD drive circuit portion. In Figure 10 of Yabe, the switching and delay circuit 34 is clearly located directly between the "processing portion" of the circuit and the endoscope proper. The description at column 8, lines 35-50 of Yabe states: "When the connector section is connected to control device 2, the matching circuit and delay circuit 34 are connected to CCD drive circuit 14 and sample-and-hold circuit 16. "This clearly teaches a system in which the matching circuit and delay circuit are part of the endoscope proper. This is directly contrary to the present invention.

In summary, therefore, the prior art of record does not teach -- regardless of whether it is taken singly or in combination -- the delay circuit of the present invention which is part of the first microprocessor and so located relative to the CCD drive circuit and the incoming signal, as

to provide the functionality that is recited in claim 1, which allows the same basic processor system to be utilized with many different endoscopes.

Claim 1, particularly as amended, is clearly distinguishable over the prior art.

Each of the dependent claims in the application contains all of the limitations of its base claim and adds further limitations which distances it even further from the prior art. For example, regarding claim 3, the Examiner takes official notice that programmable delay circuits are known. That observation, however, avoids the issue. In the typical situation, one would provide a less complicated delay circuit which is explicitly tuned to the particular needs of a particular endoscope. The provision of a programmable delay circuit that is also part of the first microprocessor, represents an additional step or feature which contributes to the overall non-obviousness of the invention. These remarks are also applicable to claims 6, 7, 8 and 12. Regarding claims 9 and 13, Nakamura discloses a control CPU that has no nexus to the problem that is solved by the present invention. Rather, in recognition of the fact that different devices may have different display systems, Nakamura discloses a control CPU that adapts itself to different display systems. Relative to claims 10 and 11, the Examiner states that the features thereof are obvious, without specific citation of prior art.

Relative to claim 4, applicant notes that the tertiary reference Pasqualini, has no nexus to endoscopes or the like. This reference deals with the peculiarities and needs of setting up signals that need to be clocked into a digital flip flops or the like. It is also important to note that in claim 4, applicant provides a multi-stage buffer circuit that is connected in series, and provides a circuit for selecting the number of stages of the buffer circuit. The latter circuit feature is not described in Pasqualini. Rather, it appears from column 8, beginning at line 61, that the actual delay is obtained by "tapping", i.e., connecting the output to a specific drive stage in the delay line. This seems to be a hardwire solution, and not a software solution type in the form of the selection circuit of the present invention described in claim 4.

Furthermore, applicant is of the opinion that a person having ordinary skill in the art would not find the need and would not be motivated to combine the Nakamura and Yabe references to arrive at the present invention on the basis of their disclosures. In this regard, please note that in Figure 1 of the Yabe reference, the "second drive signal 13" pointed out by the Examiner, is in fact the control circuit 13, which does not correspond to the "second drive signal

generator portion for generating a second drive signal for controlling a timing when the video signal extraction portion obtains the video signal from the imaging signal", as in the present invention.

Also, it is noted that the delay circuit (Figure 1, 18) pointed out by the Examiner, drives the timing generator 17 and the sample-and-hold circuit 16, which is not at all related to the CCD drive circuit, as the first drive signal generator.

It is noted furthermore, that the matching circuit & delay circuit 34 shown in Figure 10 of Yabe is provided at the connector 7 of the endoscpe cable cord 6, i.e., the endoscope itself, which is quite different from the constitution of the present invention, which recites "a delay circuit, which is stored in the first processor,...".

For all the foregoing reasons, it is respectfully submitted that the all claims of record are patentable over the prior art.

Accordingly, the Examiner is respectfully requested to reconsider the application, allow the claims as amended and pass this case to issue.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 11, 2003:

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